Frequently Asked Questions
B4655A FPGA Dynamic Probe

Data Sheet

FAQ

This document addresses common questions whose answers are not found in the FPGA dynamic probe data sheet available at **www.agilent.com/find/FPGA**.

Agilent's FPGA dynamic probe provides greater real-time measurement productivity for logic-analysis based validation of FPGAs and the surrounding system. The tool features:

- **Increased visibility** —Traditional logic analyzer probes limit engineers to measuring signals at the periphery of the FPGA. With Agilent's FPGA dynamic probe, engineers are able to measure up to 64 internal FPGA signals for each external FPGA pin dedicated to debug.

- **Faster probing changes** — Agilent's FPGA dynamic probe enables your design team to move probe points internal to the FPGA with a mouse click — without any design changes and without any changes to the timing of your design.

- **Automatic setup of the logic analyzer** — The FPGA dynamic probe maps internal signal names from your FPGA design tool to your logic analyzer. The signal-naming capability of the Agilent FPGA probe eliminates mistakes and saves you the time it would take to manually set up signal and bus names and logic analyzer connections, providing a significant advantage over logic analyzers without this capability.

Q1 How do I create an ATC2 core?

Xilinx ChipScope Pro provides the capability to create an ATC2 core. You need Xilinx ChipScope Pro to create the ATC2 core and to merge it with your design. ChipScope Pro includes Core Generator and Core Inserter. Using either of these tools, you can specify the parameters of the ATC2 core and specify which design signals go to the ATC2, making them available for real-time measurement.

Q2 How do I get an ATC2 core into my design?

Xilinx Core Inserter puts the core into your FPGA design post synthesis. Agilent recommends using Core Inserter. If you use Xilinx Core Generator, the tool instantiates your parameterized ATC2 as a black-box Verilog or VHDL unit. The synthesis tool puts the instantiated core into your design during the synthesis process.

Q3 What synthesis tools can I use to get the ATC2 core into my design?

ATC2 cores produced by Xilinx Core Generator are compatible with:

- Exemplar Leonardo Spectrum
- Synopsys Design Compiler
- Synopsys Design Compiler II
- Synopsys FPGA Express
- Synplicity Synplify
- Xilinx XST

Q4 Are there advantages to using Core Inserter versus Core Generator?

Yes. Core Inserter also produces a .cdc file. This is a small file listing the signal inputs to the ATC2 core. This file is used to automatically synchronize design signal names with logic analysis bus and signal names. Agilent recommends using Xilinx Core Inserter so you can take advantage of signal-name mapping.

Xilinx has a stimulus core known as VIO. This core can only be created and placed in a design using Core Generator. For a single design that contains both a VIO core and an ATC2, Core Generator must be used.

Q5 Core Generator does not produce a .cdc file required for automated signal name entry in the logic analyzer. If I use Core Generator instead of Core Inserter is there a way for me to manually make my own .cdc file?

Yes. You have two different options.

1. Run core generator and set the core parameters. Core Generator will make a .cdc file that you can use as a template. Open the .cdc file template using a text editor. Modify the bank input signal names so that they reflect the signal path name of the probed net.

2. The FPGA dynamic probe application read core parameters via JTAG when the user initiates a JTAG communication session with the “Connect Cable” button. One of the parameters the logic analyzer reads is the number of signal banks, and the number of signals per bank. The logic analyzer application uses generic names for each signal when a .cdc file is not loaded. For example signal 0 is generically labeled as ATC – 0 (Agilent Trace Core bit 0). On the logic analyzer, you can manually rename each ATC name with the signal names from your design. The FPGA dynamic probe application will remember name changes you made for each bank.

Q6 How big is the core? How many of my device resources does it take?

Each input signal adds roughly 1 slice to the size of the ATC2 core. The ATC2 cores have been designed to be as small as possible. For example, an ATC2 state core configured with 8 signal banks and 80 signals per bank consumes about 94 slices, or less than 1 percent of the resources on a Xilinx XCV2000 device.

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The actual core size depends on the following 3 parameters:
1. Core type: state, state with pin compression or timing
2. Number of pins
3. Number of signal banks.

Xilinx recommends measuring core sizes in terms of flops and LUTs as this is what the place and route tools work with. A formula to determine LUT and flop resource utilization from the combination of the ATC2 core and ICON (JTAG controller) is available at
http://www.agilent.com/find/fpga

Q7 Why do I see flip flops in the timing core?

The path from the probed signal to the output pad is not registered in the timing core. This path has only a combinatorial mux connected to output pads. The flip flops in the timing core are used only for core control and status. An example of a core control signal is the bank mux select. These control and status flip flops are registered by the JTAG TCK clock, not a design clock. Therefore these flip flops are part of the low-speed circuit used by the logic analyzer to control and poll the core.

Q8 Do I pay royalties for the use of the core?

No. ATC2 cores are distributed as part of Xilinx ChipScope Pro. There are no associated royalties.

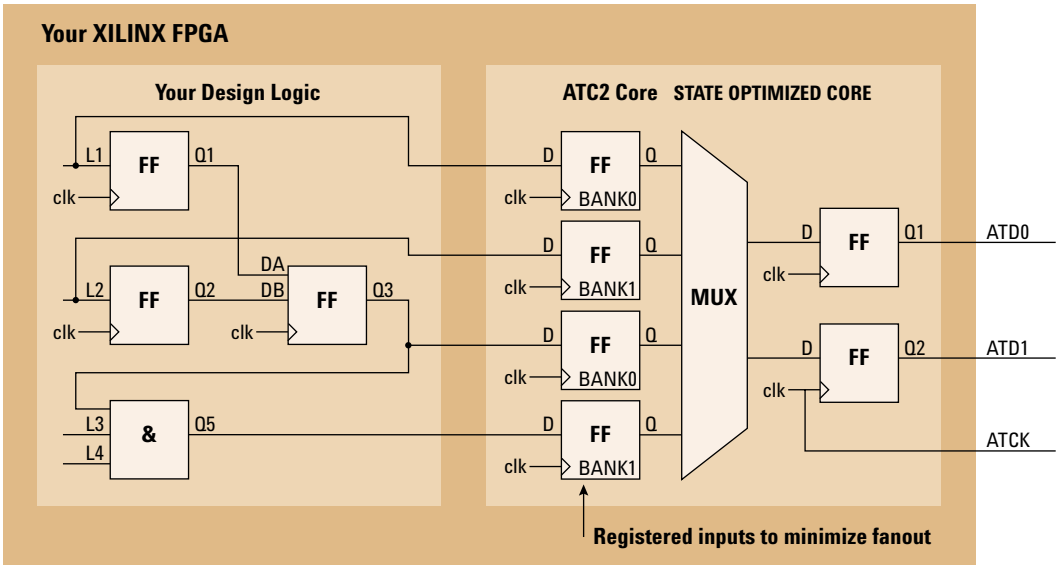
Q9 Should I leave the ATC2 core in my design after validation is complete?

This decision is up to you. Many designers prefer leaving debug cores in the design, as removing the cores from the design will change design timing. The core also can be useful for doing debug once units are in the field, if needed. The ATC2 core is by default “turned off,” and it wakes when an Agilent logic analyzer communicates with it. This feature saves power when you leave the core in a finished design.

Q10 When would I want to use an ATC2 state core (synchronous) versus a timing (asynchronous) core?

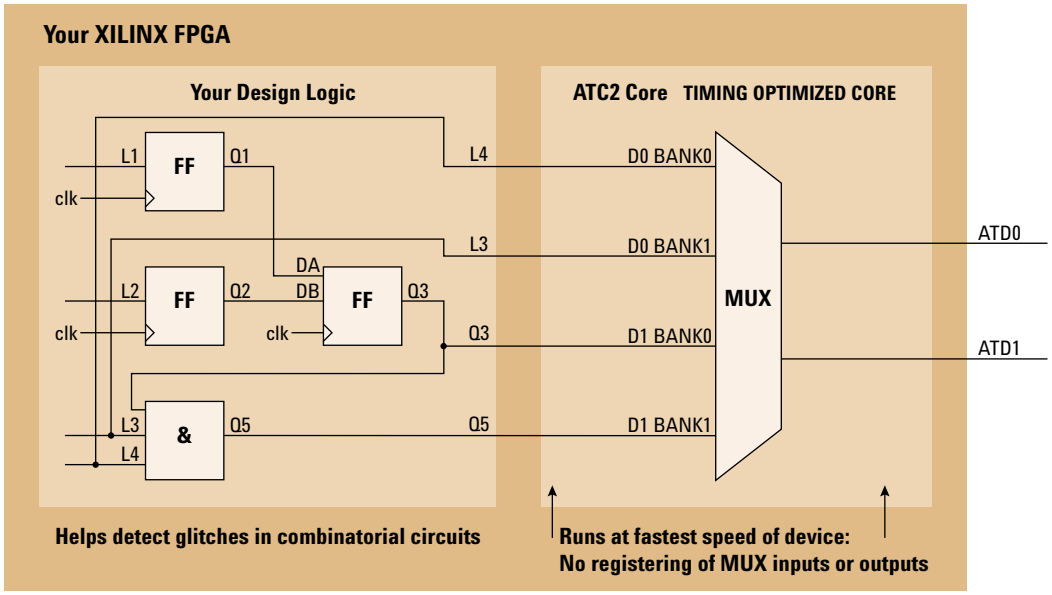
State cores:

- Provide most-accurate measurements for functional debug in one time domain
- Register inputs to minimize fan out
- Support time division multiplexing for 2X pin reduction
- Support calibration for more accurate measurements on buses with narrow data valid windows



Timing cores:

- Are best for measurements across multiple time domains
- Run at fastest-possible speed of device, no registering of MUX inputs or outputs
- Have minimal impact on design timing



Q11 What effect does the core have on my design's timing? After loading the ATC2, does it affect my signal routing?

The ATC2 core is a firm core. The core will not affect the synthesis of the design when you create and insert the design using Core Inserter. The inclusion of ATC2 core in the design may affect the placement and routing of the overall FPGA design. In typical applications, the effect should be small. The effect on design timing will depend on how the core is configured (for example, the number of signals you choose per bank, and the total number of banks) and the number of resources available on the particular FPGA device being used.

State core: The ATC2 state core includes a flop that registers data. The ATC2 core adds one additional load (flop) on each signal probed. This load will be factored into routing to meet user-specified timing constraints. This flop helps the tools meet timing constraints for most types of designs.

Timing core: The ATC2 timing core adds a wire load for each signal probed. This wire load is a false path that is ignored during place and route of the design. Hence, the timing core has minimal-to-no effect on design timing. You can determine the skew between signals by viewing the delay file generated by the design tools to estimate this difference.

Once the ATC2 core (either state or timing core) is in the design, switching from signal bank to signal bank does not change design timing, as all connections have been already made.

Q12 What's the impact on FPGA performance?

The core will have some effect on performance, but it should not be significant. The effect on performance is directly related to timing constraints. The timing core is capable of running at the fastest internal FPGA speed of the device you are using. For the timing core, the sample rate on the logic analyzer will determine how often data is captured. For state cores, the maximum sample rate will be the lower of the speed of the FPGA time domain being measured or the maximum state speed of the logic analyzer. All supported logic analyzers have state speeds of 200 MHz and greater.

Q13 How does the optional 2X pin compression technology work?

All signal inputs to the ATC2 state core are registered and clocked on the edge you specify. Internal to the core, the registered value of signal 1 is passed to the logic analyzer on the rising edge of the clock, and the value of signal 2 is passed to the logic analyzer on the falling edge of the clock. The logic analyzer uses a demultiplexing mode to decompress the information and preserve all triggering and analysis capabilities.

Q14 If I have ATC2 signal banks with 64-bit width, how many pins and logic analyzer channels does it take with 2X pin compression turned on?

Simultaneous measurement of 64 signals requires 32 FPGA pins and 64 logic analysis channels. Only 32 of the logic analysis channels are physically connected to pins of the FPGA. The other 32 channels provide their acquisition memory and triggering resources for the measurement.

Q15 Can I simulate the ATC2 core?

No. Agilent guarantees that the ATC2 core meets specifications and characteristics listed in our data sheet. The core has been debugged and tested by Agilent.

Q16 How much does the Agilent FPGA dynamic probing solution cost?

The Agilent FPGA dynamic probing technology costs $995 for a 1-year license and 1 year software update service and support. Or, a user can purchase a perpetual license and 3 years of software support and update services for $3000.

Q17 Can I use FPGA dynamic probe with multiple logic analyzers?

The FPGA dynamic probe is licensed to a single logic analyzer (1680 Series, 1690 Series, or 16900 Series). Specifically, for 16900 Series mainframes or split 1680/90 Series analyzers, multiple instances of FPGA dynamic probe are provided so you can use a single license for all logic analysis modules in the mainframe.

Q18 How will I be notified that my license is about to expire?

The 1-year license includes a 1-year software update service. This service includes FPGA dynamic probe software updates. An email notification will be sent to the address given at the time of software update service subscription.

Q19 Who do I contact if I'm having problems?

Xilinx provides ChipScope Pro expertise, including expertise on inserting the core into your design. Agilent's expertise is on the core and FPGA dynamic probe application. Agilent and Xilinx work together on issues that cross company boundaries.

Q20 What if I didn't assign all of the signals of interest early when I created the core?

You can still use Xilinx FPGA editor to route new input signals to the ATC2 core. However, a new .cdc file is not produced, so you will need to by updating the new signal name on the logic analyzer. Alternatively, you can change input signals by recompiling the FPGA design with a new ATC2 core or new signal connections to the core.

Q21 If I use FPGA editor, the signals being presented to the logic analyzer are now different from what the .cdc file specified. What can I do to reflect my design changes?

On the logic analyzer, you can manually rename whatever signal names you need to. In the FPGA dynamic probe application, simply activate the bank where the signal name change is needed. Then in the logic analyzer setup, listing, or waveform menu, modify the previous signal name with the new one you have routed out with FPGA Editor. The FPGA dynamic probe application will remember name changes you made for each bank signal.

Q22 Can I use the FPGA dynamic probe application to download configuration bits into my Xilinx FPGA?

Yes.

Q23 What Xilinx JTAG cables work with FPGA dynamic probe?

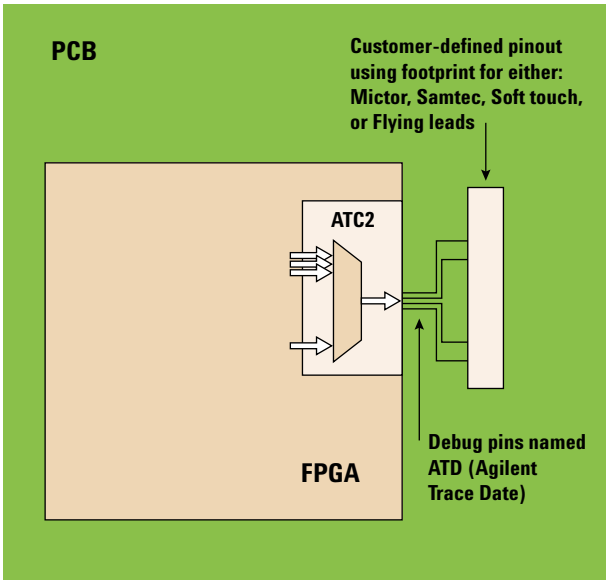
Xilinx Parallel III cable and IV MultiLINX cables. The cable makes a connection between the parallel port on the logic analyzer and the JTAG pins on the FPGA being measured.

Q24 Does the FPGA dynamic probe work if I have non-Xilinx devices on the scan chain?

Yes. The application can handle up to 256 devices in a scan chain. The devices can be Xilinx or non-Xilinx devices. When a non-Xilinx device

is found, dynamic probe will ask for the JTAG IR length. This value is readily available from the chip manufacturer. The application saves this value and uses it when communicating with your scan chain.
When the application needs to talk to a selected Xilinx FPGA device, it puts all devices into bypass mode except for the selected device. BYPASS mode is a JTAG required function in which the device simply adds a flop delay between TDI data to TDO. When in bypass the data is ignored by the BYPASS-ed device and it operates as it normally does (for example a microprocessor keeps running user code).

One thing to keep in mind is that Xilinx's parallel programmer hardware may not support driving 256 devices in one scan chain. In particular the TCK and TMS lines are heavily loaded when JTAG is configured as a chain. The reason is that the cable will drive TCK and TMS to all devices in a scan chain. For this reason you should consider buffering these signals on you board if you have more than 6 devices in a scan chain (simple rule of thumb). One other thing you can do if you have more than 6 devices or are simply having problems connecting to your FPGA simply lower the JTAG TCK speed. With dynamic probe you can select from various speeds down to 200KHz as a TCK rate. By slowing down TCK you will increase the setup/hold margin for TMS on all devices and TDI on the first device.



Q25 How does calibration work?

The core contains test generation circuitry to stimulate the signal banks and output pins. With this active data running, the logic analyzer invokes the Eye Finder feature to automatically adjust for variances in path delays through the core to the acquisition system on the logic analyzer.

Q26 Can I use the calibration feature with an ATC2 timing core?

No. Calibration works exclusively for ATC state analysis cores.

Q27 Can I use a different clock on each bank or do I need a clock with each bank?

Timing cores do not have a clock, because information is sampled using the logic analyzer's internal clock. For state cores, the ATC2 core has a master clock that is used for all banks.

Q28 Can I put multiple ATC2 cores in a single device?

Yes. The FPGA dynamic probe application has been architected to support multiple cores in a single FPGA device. If the cores are state cores, each will need a clock from the design it is measuring.

Q29 Can I map two cores in a single physical probe?

Yes. For example the first ATC2 core with 16 output pins could be mapped to the outside of mictor connector with its corresponding clock. A second ATC2 core with five output pins could be mapped to the even side of the same mictor connector. A separate logic analysis module is required to collect acquisition data for each core.

Q30 Which Xilinx FPGAs are supported?

FPGA dynamic probe supports Xilinx Spartan-3, Virtex-II, and Virtex-II Pro FPGAs.

Q31 What triggering resources are available with the FPGA dynamic probe?

The full trigger resources of the Agilent logic analyzer being used are available.

Q32 What special pinouts are required by FPGA dynamic probe?

No special pinouts are required. The FPGA dynamic probe includes a graphical feature called pin mapping. This feature lets you visually tell the tool how the FPGA physical pins that carry the MUX output (ATD – Agilent Trace Data) are connected to the logic analyzer. If you are using a traditional probing connection, such as a Mictor or Samtec connector, or a soft touch probe, the graphic lets you specify the location of each ATC2 output and which logic analysis cable is connected to this probe.

Q33 How much skew exists between internal FPGA signals that are routed through the ATC2 state core and an external bus measurement on my PC board?

ATC2 state cores are synchronous and contain pipelining. The ATC2 state core uses 2 levels of pipelining before the signal is passed to the logic analyzer. For an ATC2 state core with pin compression, there are 4 levels of pipelining. The skew will be equal to the clock period times the number of pipeline levels.

Q34 When you select names of nets to probe in Xilinx Core Inserter, do you select from the post-synthesis net names or the original RTL names?

The signals names that Xilinx Core Inserter has access to are from the post-synthesis netlist. If there is an RTL name that you want to make sure doe not get optimized out, you can use a command such as Synplicity's SYNKEEP to preserve RTL signals.

Q35 Can I debug and probe at the RTL level, like Synplicity's Identify product?

No, the Xilinx Pro Core Inserter currently works at the signal & bus level.

Q36 Can I debug using FPGA dynamic probe with a design that has been instrumented using Synplicity's Identify product?

Yes. Each tool can be used sequentially, but not at the same time. Both tools require control of the JTAG scan chain and thus only one can be used at a time.

Q37 Should I synthesize my FPGA design in one pass or hierarchically?

When selecting signal names for probing using Xilinx Core Inserter, the tool works best with a "flattened" design that was synthesized all at one time. If you have a hierarchical design, Core Inserter lets you select signals from the top level of the design.

Q38 Can I feed an external clock in for a State measurement with a State core?

Yes, but this external clock would need to also drive the FPGA internal clock for the timebase being observed in order for the measurements to make sense. For example, you could use an external pulse generator, and feed it into the FPGA as a clock, and feed it into the clock input of the logic analyzer.

Q39 Can I sequentially use ChipScope Pro ILA and FPGA dynamic probe (ATC2 core) on a design using the same JTAG cable?

Yes. There are two options. If you install ChipScope Pro on the Agilent logic analyzer this application will communicate via the JTAG cable connected to the parallel port on the logic analyzer. The FPGA dynamic probe application also uses this same port and can "share" the cable. A user can toggle back and forth between the software application without making any cable or JTAG modifications as both applications use the same drivers for cable communication. The second option is to install ChipScope Pro on a standalone PC. In this case you can move the cable from the logic analyzer parallel port to the equivalent port on the PC when you are using ChipScope Pro. Move the cable connection back to the logic analyzer parallel/USB port when you want to use the FPGA dynamic probe. (Note, in the second scenario the application which doesn't have direct cable access will not be able to take new measurements until the cable is connected.)

General questions on purchasing and installing ChipScope Pro tools

Q40 What is ChipScope Pro?

ChipScope Pro is the on-chip verification and debug tool for Xilinx FPGAs including:

- ILA core and ChipScope Pro Analyzer (not used in FPGA dynamic probe application)
- Core Inserter
- Core Generator

Q41 What Xilinx FPGA devices do ChipScope Pro tools support?

ChipScope Pro tools support; Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, Spartan-II, Spartan-IIE, and Spartan-3.

Q42 Is ChipScope Pro sold as a time-based license agreement?

Yes, ChipScope Pro is sold under the standard Xilinx one-year time-based license agreement.

Q43 What do I get when I purchase ChipScope Pro tools?

You will receive a letter with a ChipScope Pro product ID and instructions on how to access ChipScope Pro tools including the ChipScope Pro Core Generator and Core Inserter, ChipScope Pro Analyzer, and ChipScope Pro soft cores (ILA, IBA, VIO), as well as the Agilent ATC2 core.

Q44 How can I get the latest version of ChipScope Pro tools?

You can get the latest version of ChipScope Pro tools online at
http://www.xilinx.com/ise/verification/cs_pro_get.htm

Q45 Is there an evaluation version of ChipScope Pro tools?

Yes, there is a full-featured 90-day evaluation version of ChipScope Pro tools that is available for download at
http://www.xilinx.com/ise/verification/cs_pro_get.htm

Questions on using ChipScope Pro tools

Q46 What is the ChipScope Pro Core Generator?

Similar to the ISE CoreGen tool, the ChipScope Pro Core Generator allows you to define parameters for ChipScope Pro cores, and generates synthesizable HDL that can be combined within your design.

Q47 What is the ChipScope Pro Core Inserter?

The ChipScope Pro Core Inserter allows you to add ChipScope Pro cores after the design has been synthesized by merging design netlists.

Q48 What is the ChipScope Pro Analyzer?

The ChipScope Pro Analyzer is the main interface that allows you to configure Xilinx FPGAs, find ChipScope Pro cores within a design, and set up and define trigger conditions. The ChipScope Pro Analyzer is similar to a logic analyzer, in that it allows you to view and interact with data captured for the purposes of debug and verification.

Q49 What is ChipScope Pro ILA?

ChipScope Pro ILA (Integrated Logic Analyzer) allows you to view signals and nodes within the Virtex-II Pro FPGA design. Multiple trigger inputs, trigger sequencing and optional time stamping allow you to better utilize the available block RAM within your device under test. The ILA cores communicate via JTAG with the ChipScope Pro Analyzer.

Q50 What is ChipScope Pro IBA?

ChipScope Pro IBA (Integrated Bus Analyzer) is the industry's first integrated bus analysis core. ChipScope Pro IBA is a CoreConnect-specific bus analyzer that allows you to capture and display transaction and signal activity between the PPC405 processor and IP components in the FPGA fabric.

Questions on Xilinx and Agilent on-chip debug solutions

Q51 What is the Agilent Xilinx relationship?

Teams within Agilent and Xilinx have worked closely together over the past several years to provide solutions for on-chip debug of Xilinx FPGAs. These solutions have become part of the Xilinx ChipScope Pro solution.

Q52 What is the status of the Xilinx/Agilent trace port analyzer solution?

The Agilent FPGA trace port analyzer solution, introduced just over a year ago, will be discontinued on October 31, 2004. The capabilities available in the Agilent FPGA trace port analyzer solution have been improved and are now available in a new technology known as FPGA dynamic probing from Agilent.

Q53 Will the Agilent trace port analyzer continue to be supported?

Yes, ChipScope Pro tools and Agilent will continue to support the Agilent trace port analyzer solution, although customers will no longer be able to purchase this solution.

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Phone or Fax

United States:
(tel) 800 829 4444
(fax) 800 829 4433

Canada:
(tel) 877 894 4414
(fax) 905 282 6495

China:
(tel) 800 810 0189
(fax) 800 820 2816

Europe:
(tel) 31 20 547 2111

Japan:
(tel) (81) 426 56 7832
(fax) (81) 426 56 7840

Korea:
(tel) (080) 769 0800
(fax) (080)769 0900

Latin America:
(tel) (305) 269 7500

Taiwan:
(tel) 0800 047 866
(fax) 0800 286 331

Other Asia Pacific Countries:
(tel) (65) 6375 8100
(fax) (65) 6755 0042
Email: tm_ap@agilent.com

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